Registration Form

1. **Name:**
2. **Designation:**
3. **Institution:**
4. **Department:**
5. **Address for Correspondence:**

Mobile:

E-mail:

6. **Qualifications:**
7. **Teaching Experience (in years):**

Declaration

The information furnished above is true to the best of my knowledge.

Date:
Place:

Signature of Applicant

Approval from Competent Authority

Important Dates

Last date for the receipt of applications:
3rd October 2015
Date of intimation regarding selection:
4th October 2015
Confirmation by participants:
4th October 2015
Certificate will be issued to all the participants.

Registration Fee

No registration fee will be charged

Please confirm your participation through mail. A scanned copy of the duly filled application forms are to be sent to:

Dr. Jasdeep Kaur Dhanoa
Associate Professor
Department of E & C Engg.
IGDTUW, Delhi
Email: nittr.igdtuw@gmail.com

Dr. Nidhi Goel
Associate Professor
Department of E & C Engg.
IGDTUW, Delhi
Email: nittr.igdtuw@gmail.com

ICT Based
One Week Program
on
VLSI DESIGN
(05th – 09th October 2015)

Course Coordinator
Dr. Rajesh Mehra
Associate Professor, NITTTR- Chandigarh

Co-ordinator
Dr. Jasdeep Kaur Dhanoa
IGDTUW, Delhi

Deputy Co-ordinator
Dr. Nidhi Goel

Organizing Committee
Ms. Vandana Niranjan
Ms. Veepsa Bhatia
Dr. Richa Yadav
Ms. Shobha Sharma

Organized by
Dept. of E & C Engg.
IGDTUW- Delhi
In Association with
NITTTR, Chandigarh

About the College

Indira Gandhi Delhi Technical University for Women (IGDTUW) is a non-affiliating teaching and research University at Delhi to facilitate and promote studies, research, technology, innovation, incubation and extension work in emerging areas of professional education among women, with focus on engineering, technology, applied sciences, management and its allied areas with the objective to achieve excellence in these and related fields.

The objective of the University is to foster industry relevant research and innovations and empower the women of our country through value based higher education making them employable, self reliant, responsible citizen of the country with concern for environment and society.

About the Department

The Department of Electronics and Communication Engineering, IGDTUW has been known for its exceptionally strong Under-Graduate and Post Graduate programmes. It has been dedicated to provide dynamic and quality women engineers to the industry and society. The Department offers one Undergraduate (UG) and two Postgraduate (PG) programmes, M. Tech in VLSI Design and M. Tech (ECE) Part-Time course. The Department has always been on a high growth path and has an experienced and dedicated faculty with a strong commitment to engineering education. The Department, offers strong research orientation to students in the areas of Communication Systems, Signal and Image Processing, Embedded systems, Microelectronics and VLSI Design.

About the VLSI Design Program

The main objective of this program is to provide an opportunity to faculty members and research scholars to enrich knowledge and enhance their professional growth by acquiring knowledge from various specialists from both industry and academia.

It will give an overview to the participants on digital and analog design simulation, low power and nanoscale VLSI Design, device modeling and interconnect design.

This workshop will be beneficial for the participants who are interested to learn and cultivate new thoughts in the field of Microelectronics.

This workshop will comprise of lectures delivered by experts from IIT Roorkee, IIT Ropar, NIT Kurukshetra, NIT Hamirpur, NTTTR Chandigarh and design engineers from Semiconductor Laboratory , Mohali , Cadre design system, New, Delhi & Entuple technologies, New Delhi.

The following topics will be covered in the workshop:-

- CMOS Design Overview
- Digital Design Simulation Analog CMOS Design
- Advance MOSFET
- 3D Device Modeling
- Low Power VLSI Design
- Verilog Based VLSI Design
- Analog Design Simulation
- High Performance CMOS Design
- VLSI Interconnect Design Issues
- High Speed Interconnects
- Novel Multigate Transistors
- Nano-Scale VLSI Design

Venue

Seminar Hall (Electrical Block)
Department of Electronics Engineering,
IGDTUW
Kashmere Gate, Delhi-110006

Resource Persons

- Dr. Rajesh Mehra (NITTTR Chadigarh)
- Dr. Anand Bulusu (IIT Roorkee)
- Dr. Rajeevan Chandel (NIT Hamirpur)
- Dr. R.K. Sharma (NIT Kurukshetra)
- Dr. Rohit Sharma (IIT Ropar)
- Er. H S Jatana (Mohali, Punjab)
- Er. Deep Sehgal (Mohali Punjab)
- Er. Amit Saini (CADRE Design Sys., Delhi)
- Er. Varun Bhadana (ENTUPLE Tech., Delhi)